Low-voltage high dynamic range CMOS exponential function generator

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Abstract:
A low-voltage low-power analog CMOS exponential function generator is designed in 0.18µm CMOS standard technology. The proposed circuit uses Taylor’s approximation concept and consists of a linear low-voltage transconductance with two linearization techniques and one low-voltage current squarer circuit for performing this approximation method. Simulation results using HSPICE shows 60 dB-linear output current range with the linearity error less than ± 0.5 dB. The total power consumption is below 0.14mW with a single 1 V power supply.

Keywords: Exponential function generator- Low-voltage-V-I converter

1. Introduction

The exponential function generator is essential and important building block in a variable gain amplifier (VGA) [1]. However, unlike the BJT device, there is no intrinsic logarithmic device working in saturation for CMOS technologies. For overcoming this problem one method is to generate the exponential characteristics by using of a “pseudo-exponential” generator [1-3]. Alternatively, The Taylor series expansion can also be used for implementing the exponential function [4-7]. For applying the Taylor concept, the dB-linear V-I Converter have to be implemented by using the composition of a V-I squarer circuit, a linear V-I converter and a constant bias current [4-6], or by using composite NMOS transistors [7]. However, these previously reported structures show very small dB-linear variation of the output current (less than 15 dB with a linearity error less than ± 0.5 dB) [6,7]. Moreover, these structures are not power efficient (0.9 mW) and operate at high supply voltage (3V) [6,7].

In this paper a low-voltage high-linear exponential function generator is presented. The proposed circuit uses the current-to-current squarer and low-voltage V to I transconductance with new linearization technique so that the circuit can operate at very low voltage application. In section 2, the block diagram of proposed circuit is explained. V to I transconductance and current-to-current squarer circuit are shown in section 3 and simulation results are presented in section 4. Finally, conclusion is made in Section 5.

2. The proposed block diagram

According to the Taylor’s series expansion, a general exponential function can be expressed as

$$e^{ax} = 1 + \frac{ax}{1!} + \frac{(ax)^2}{2!} + \frac{(ax)^3}{3!} + \cdots$$ (1)

Where $a$ and $x$ are the coefficient and the independent variable, respectively. For $|ax| << 1$, the Eq. (1) can be approximated as

$$e^{ax} \cong 1 + \frac{ax}{1!} + \frac{(ax)^2}{2!}$$ (2)

For $|ax| < 1$, the Eq. (2) provides 14 dB variation and 12 dB linear variations with the error less than ± 0.5 dB. A new function block diagram to realize the squaring function of Eq. (2) is given in Fig. 1, which also includes the transfer function of all blocks.
The output current \( I_{\text{lin}} \) of the linear V-I converter, which is a function of \( V_d = V_{\text{in}+} - V_{\text{in}-} \), is multiplied by \( K_1 \) and \( K_2 \) to generate two current signals \( K_1I_{\text{lin}} \) and \( K_2I_{\text{lin}} \), respectively. The \( K_2I_{\text{lin}} \) goes to the Current squarer and then is added to the other signal \( K_1I_{\text{lin}} \) to form the Eq. (3).

The output current as an approximated exponential function is given as

\[
I_{\text{OUT}} = 2I_0 + K_1I_{\text{lin}} + \frac{K_2^2I_{\text{lin}}^2}{8I_0}
\]  
(3)

\[
I_{\text{OUT}} = 2I_0 \left( 1 + \frac{K_1}{2I_0} + \frac{K_2^2I_{\text{lin}}^2}{16I_0^2} \right)
\]  
(4)

Where \( I_0 \) is the bias currents of the current squarer [8]. To satisfy the condition of exponential function as in Eq. 1, the coefficient \( a \) and the independent variable \( x \), have to satisfy the following condition

\[
\frac{K_2}{K_1} = \sqrt{2} \quad \text{and} \quad a = \frac{K_1}{2I_0}
\]  
(5)

From Eq. (4), the exponential characteristic is easily achieved by setting the multiplying factors \( K_1 \) and \( K_2 \). Also, the symmetrical-axis is controlled by \( K_1 \) and \( K_2 \). The multipliers are actually current mirrors. Hence, \( K_1 \) and \( K_2 \) are achieved by setting transistors’ size in the current mirrors. The other advantage of this method is that the transconductance of the exponential V-I converter can be tunable easily by adjusting the bias current \( I_0 \).

### 3. V to I transconductance circuit

Considering quadratic \( i - v \) characteristics for the MOS transistors and neglecting the channel length modulation effect, the simple differential MOS transconductor has a transfer characteristic given by

\[
i_i = \sqrt{2kI_0v_i} \sqrt{1 - \frac{v_i^2}{8I_0}}
\]  
(6)

Where \( k \) represents the transconductance parameter \( (k = \mu C_{\text{ox}} \frac{W}{L}) \).

Better linearity can be achieved for large effective gate-to-source voltages \( V_{\text{GSeff} = V_{\text{GS}} - V_{\text{TH}}} \). For low-voltage applications this constitutes a major drawback. Furthermore, large transconductance values can be obtained only by using large bias currents and large area transistors; however this changes cause to enlarge the power consumption and active area.

One of the topologies for linearization of the transfer characteristic of MOS transconductors is using the adaptive biasing current source.[11]

The idea is using a dynamic bias current containing an input dependent quadratic component to cancel the nonlinear term in equation (6). Hence, if the bias is defined as equation (7),

\[
I_o = I'_o + \frac{kV_i^2}{8}
\]  
(7)

And put this equation in equation (6) the transfer characteristic becomes linear and could be realized according to equation (8)

\[
i_i = \sqrt{2kI'_o}v_i
\]  
(8)

### 3.1 The novel low-voltage circuit for generating the adaptive bias current

Fig. 2 shows the new low-voltage circuit for generating the adaptive bias current.
Assuming the same sizes for M1, M2, it can be easily shown that:

\[ I_1 = \frac{1}{2} k_1 \left( V_{cm} + \frac{V_i}{2} - V_{th} + V_{GSb} - V_{thb} \right)^2 = \frac{1}{2} k_1 \left( \frac{V_i}{2} + V_{GSb} - V_{thb} \right)^2 \]  

(9)

Where \( k_1 \) is the transconductance parameter of input devices, M1 and M2, \( k_1 = k_2 = \mu_{Cox} \frac{W_1}{L_1} \)

Similar attempt for I2 terminates to equation (9):

\[ I_2 = \frac{1}{2} k_2 \left( -V_i + V_{GSb} - V_{thb} \right)^2 \]  

(10)

Replacing \( V_{GSb} \) as a function of the bias current \( I_b \)

\[ V_{GSb} = V_{th} + \sqrt{\frac{2I_b}{W_b \mu_{Cox}}} \]  

(11)

The following expression result:

\[ I_1 = \frac{1}{2} k_1 \left( \frac{V_i}{2} + \sqrt{\frac{2I_b}{W_b \mu_{Cox}}} \right)^2 \]  

(12)

\[ I_2 = \frac{1}{2} k_2 \left( -\frac{V_i}{2} + \sqrt{\frac{2I_b}{W_b \mu_{Cox}}} \right)^2 \]  

(13)

The current passing through MC is equal to the sum of I1, I2 and Ib as clarified in equation (14):

\[ I_c = I_1 + I_2 + I_b = I_b + \frac{1}{2} k_1 \left( \frac{V_i^2}{2} + \frac{4I_b}{W_b \mu_{Cox} \frac{W_b}{L_b}} \right) \]  

(14)

As seen in (14), the current of MC is related in quadratic relation with the input differential voltage.

If a copy of the current of MC is mirrored into the tail current of basic differential pair which is discussed former in section 2.1, equation (15) can be concluded from combination of equations (6) and (14):

\[ i_o = \frac{1}{2} k v_i \left[ \frac{8}{k} I_b + \frac{16 k_1}{k k_b} I_b + \frac{2 k_3}{k} V_i^2 - V_i^2 \right] \]  

(15)

Where \( k = \mu_{Cox} \frac{W}{L} \) is the transconductance of basic differential pair, \( k_1 = \mu_{Cox} \frac{W_1}{L_1} \) is the transconductance of adaptive biasing differential pair and \( k_b = \mu_{Cox} \frac{W_b}{L_b} \) is the transconductance of M_b transistor. If \( k_1 = 0.5 k \) the transfer characteristic becomes completely linear according to relation (16):

\[ i_o = \frac{1}{2} k v_i \left[ \frac{8}{k} I_b + \frac{8}{k_b} I_b \right] \]  

(16)

### 3.2 The novel linear MOS transconductor

We proposed a new MOS transconductor that uses the linearization approach presented above. The proposed circuit consists of 3 main blocks; an adaptive biasing current generator, a high performance current mirror and a main differential pair (fig. 3). M_{C1}-M_{C4} Formed a high performance current mirror. [12] This circuit copy the dynamic current that produced by Adaptive bias current generator circuit which formed by Ma1, Ma2, Mb and
Mc into the source of the transistors of main differential pair with source degeneration transistor which formed by M₁- M₂.

![Diagram](image)

Fig. 3. The novel linear transconductor

Mₘ, current source Iₘ, and Vₘ forces the V_DS voltage of transistor Mₐ to a constant value. A replica of this circuit is used to force the V_DS voltage of the transistor Mₐ₁ to be equal to that of transistor Mₐ.

To have high output impedance, the output cascade transistor Mₐ₄ is driven by the drain of transistor Mₐ₂. As the polarity in the drain of transistor Mₐ₂ is reversed, an inverting stage is required to drive the gates of transistor Mₐ₄. This Inverting stage provides additional gain-boosting, which increases the output impedance. The inverter amplifier has been implemented by means of transistor Mₐ₃ and biasing current Iₘ₁.

The inverter amplifier has been implemented by means of transistor Mₐ₃ and biasing current Iₘ₁. The minimum supply voltage is limited by the path formed by Iₘ, Mₘ, and Mₐ, so the minimum supply voltage is

\[
V_{DD}^{\text{min}} = V_{GSC} + 2V_{DS_{\text{sat}}} \tag{17}
\]

where \(V_{GSC}\) is gate-source voltage of Mₐ, \(V_{DS_{\text{sat}}}\) is the minimum voltage drop in current source Iₘ, and can be as small as 0.1V in 0.18μm CMOS technology, \(V_{th} = 0.55\) V for NMOS, so

\[
V_{DD}^{\text{min}} = V_{th} + 3V_{DS_{\text{sat}}} = 0.55 + 3 \times 0.1 = 0.85\text{V}
\]

We have selected \(V_{DD}=1\) V in order to have an appreciable voltage swing.

### 3.3 Current Squarer Circuit

Fig.4 shows the low-voltage current squarer circuit[8]. It can be shown that, in Fig. 6, the output current Isq is given by
Fig. 4 The current squarer circuit [8]

\[ I_{sq} = 2I_0 + \frac{K_2 I_{in}}{I_0} \] (18)

Where \( I_0 \) is the bias current as shown in Fig. 4.

4. Simulation results:

Fig. 5 shows the proposed exponential function generator. The proposed circuit consists of a low-voltage high-linear V to I converter, two adjustable current mirrors which form \( K_1 \) and \( K_2 \) and low-voltage current squarer. The proposed circuit works with 1 V power supply in 0.18 \( \mu \)m CMOS technology, in order to satisfy the condition \( |ax| << 1 \) in Eq.(2), should satisfies the condition \( |K_1 I_{in}| < 2I_0 \). The bias current \( I_{bias} \) can be adjusted to get the I-V curve that satisfies \( |K_1 I_{in}| < 2I_0 \) higher dB-linear output current range can be achieved By adjusting the \( K_1 \) and \( K_2 \).

Fig. 5 The proposed exponential function generator

Fig. 6 shows DC characteristic of proposed transconductance circuit. Note that high linearity was obtained, which was also confirmed by the total harmonic distortion. A -118 dB was obtained for a 400 mV peak to peak differential input voltage at 125 KHz. Figure. 7 shows the total harmonic distortion (THD) for different frequencies for transconductance circuit.

Fig. 8 shows the I-V characteristic for proposed exponential function generator with more than 60 dB dynamic range with the linearity error less than \( \pm 0.5 \) dB over variation of input voltage between -0.7 V to 0.7 V.
Fig. 6 Post layout simulated DC transfer characteristic for Ib from 3µA to 6µA by 1µA step

Fig. 7 Total Harmonic Distortion (THD) for different frequencies: × 1.25 MHz ; • 125 KHz

Fig. 8 The I-V characteristic of the proposed circuit

5. Conclusion
A low-voltage low-power circuit for realizing the exponential function is presented. The circuit operates at a low supply voltage (1 V). The proposed circuit combines two linearization methods to enhance the linearity. The proposed circuit achieves more than 60 dB dynamic range and can find application in the design of an extremely low-voltage and low-power VGA.

ACKNOWLEDGEMENT

The manuscript was resulted from research proposal entitled “Low Voltage High Linear CMOS Pseudo-Exponential Function Generator” which is supported by, Department of Electrical Engineering, College of Electrical Engineering, Mahshahr Branch, Islamic Azad University, Mahshahr, Iran.

Reference